WHAT IS CLAIMED IS:

1. An apparatus for providing power from a secondary power source where the secondary power source has a lower potential than a primary power source, comprising:

a field effect transistor, coupled to the secondary power source;

a first diode, coupled to the field effect transistor and to a device to be powered;

a second diode, coupled to the primary power source and the device to be powered; and

an inverter, coupled to a gate of the field effect transistor, wherein the inverter maintains the field effect transistor in a pinched-off condition and preventing a current flow from the secondary power source when the primary power source is available.

2. The apparatus of claim 1, wherein the field effect transistor is a depletion mode field effect transistor.

3. The apparatus of claim 2, wherein the depletion mode field effect transistor is an n-channel depletion mode field effect transistor.

4. The apparatus of claim 1, wherein the field effect transistor is an enhancement mode field effect transistor.

5. The apparatus of claim 4, wherein the enhancement mode transistor is a p-channel enhancement mode field effect transistor.

6. An apparatus for providing power from a secondary power source where the secondary power source has a lower potential than a primary power source, comprising:

a first diode, coupled between the primary power source and a device to be powered;

a second diode, coupled to the secondary power source;

a field effect transistor, coupled to the second diode and primary power source and the device to be powered; and

an inverter, coupled to a gate of the field effect transistor, wherein the inverter maintains the field effect transistor in a pinched-off condition and preventing a current flow from the secondary power source when the primary power source is available.

7. The apparatus of claim 6, wherein the field effect transistor is a depletion mode field effect transistor.

8. The apparatus of claim 7, wherein the depletion mode field effect transistor is an n-channel depletion mode field effect transistor.

9. The apparatus of claim 6, wherein the field effect transistor is an enhancement mode field effect transistor.

10. The apparatus of claim 9, wherein the enhancement mode transistor is a p-channel enhancement mode field effect transistor.